

IDS Form PTO/SB/08: Substitute for form 1449A/PTO

Complete if Known

Application Number 09/661,919

Filing Date September 14, 2000

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Art Unit 2128

Examiner Name F. Ferris III

Attorney Docket Number 3180.0265

Sheet 1 of 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No. <sup>1</sup>	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation <sup>8</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
		JP 9-245081	9/19/97	Nippon Telegraph & Telephone Corp.		Abstract
		JP 8-249372	9/27/96	Toshiba Corp.		Abstract
		JP 8-153127	6/11/96	Hitachi Ltd.		Abstract

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation <sup>8</sup>
		Notice of Grounds for Rejection issued by the Japanese Patent Office mailed April 11, 2006, for Japanese Patent Application No. 11-264538, and English-language translation thereof	
		UCHINO, "METHOD FOR ESTIMATING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT," Toshiba Technology Publications (August 29, 1996), 14-46:1-2	

Examiner Signature *F. Ferris III* Date Considered 5/24/06

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